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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/881,254 | 06/14/2001 | Fwu-Iuan Hshieh | GS 134 | 6677 |

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| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 02/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/881,254 | HSHIEH ET AL. | |
| | Examiner | Art Unit | |
| | Johannes P Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) 17-24 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restrictions*

Response without traverse to a restriction requirement filed 02/08/02 has been entered as Paper No. 4. Therefore, claims 1-16 as elected by Applicants have been exclusively examined.

### *Information Disclosure Statement*

The examiner has considered the items listed in the Information Disclosure Statement filed 06/14/01 which has been entered as Paper No. 2.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1 – 4, 6 – 8, and 10 – 16*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al (4,250,519) in view of Vinson (4,116,720).

*With regard to claims 1 – 3:* With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:

a drain region 27 (cf. column 3, lines 13-14) of first conductivity type (n type);

a body region 26 of second conductivity type (p type) provided over said drain region, said drain region and said body region forming a first junction;

a source region 24 (cf. column 3, lines 3-4) of first conductivity type provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region, through said body region and into said drain region (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising an insulating layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a conductive region 32 (cf. column 3, line 20) within said trench adjacent said insulating layer, and in which gate region gate metal, particularly aluminum metal (cf. column 3, line 21) is allowed to be adjacent said conductive region (the additional limitation as defined by *claim 3* is thus anticipated by Mogi et al).

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3) (the additional limitation as defined by *claim 2* is thus anticipated by Mogi et al).

*Mogi et al do not necessarily teach* the further limitation defined ad (b) in claim 1 of Applicants. *However,* in a patent on a vertical MOSFET with groove

alias trench (cf. title and abstract) and *for the specific purpose of retaining electrical symmetry (cf. column 6, line 32)*, Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer without additional doping (cf. column 3, lines 5-6 and line 24) with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include aspect ad (b) as taught by Vinson.

*With regard to claim 4:* body region 26 in Mogi et al is a lightly P-doped semiconductor (epitaxial) layer (cf. column 3, lines 5-6), any doped semiconductor region has dopants, while each dopant is a generation-recombination center. Thus the further limitation of claim 4 does not distinguish from the prior art as taught by Mogi et al.

*With regard to claim 6:* source, drain, and body regions as taught by Mogi et al are doped silicon regions (cf. column 2, line 61 – 63, column 3, lines 13 – 14 and 24). Therefore, the further limitation as defined by claim 6 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 7:* said conductive region 32 as taught by Mogi et al can be made of polysilicon (cf. column 3, lines 20-23). Therefore, the further limitation as defined by claim 7 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 8:* said insulating layer 29 as taught by Mogi et al is a silicon dioxide layer (cf. column 3, lines 22-23). Therefore, the further limitation as defined by claim 8 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 10:* the examiner takes official notice that in general, a gate insulator layer of silicon dioxide formed using CVD or PVD has many dangling bonds within the film. These become interface states or fixed charges within the insulating layer. Applicants' further limitation as defined by claim 10 is therefore a result of standard fabrication procedures of said insulating layer and does not distinguish over the prior art.

*With regard to claim 11:* said source and drain regions as taught by Mogi et al are heavily doped regions (cf. column 3, lines 3-4 and 13), while said body region 26 (cf. column 3, lines 5-6) as taught by Mogi et al is a lightly doped region. It follows that said source and drain regions have peak net doping concentrations that are greater than a peak net doping concentration of said

body region. Therefore, the further limitation as defined by claim 11 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 12:* said first conductivity type taught by Mogi et al is n type and said second conductivity type as taught by Mogi et al is p type, as detailed above in the discussion of claim 1. Therefore, the further limitation as defined by claim 12 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 13: Mogi et al do not necessarily teach* the further limitation of claim 13. *However, it has long been known* that source and drain can be made in the present art by a single irradiation by dopants, as actually taught by Vinson, who teaches the use of an ion beam *for the purpose* of exploiting ion implantation to simultaneously, hence in a cost-effective manner, create the heavily doped source and drain regions by use of the same dopant material (see Fig. 2D, and column 3, lines 42-50).

*With regard to claim 14:* With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:

a silicon drain region 27 (cf. column 2, lines 61-63 and column 3, lines 13-14) of N-type conductivity;

a silicon body region 26 of P-type conductivity (cf. column 3, lines 5-6) provided over said drain region, said drain region and said body region forming a first junction;

a silicon source region 24 (cf. column 3, lines 3-4) of N-type conductivity provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region, through said body region and into said drain region (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising a silicon dioxide layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a doped polycrystalline silicon region 32 (cf. column 3, line 20) within said trench adjacent said silicon dioxide layer,

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3). In the invention taught by Mogi et al the source and drain region have peak doping densities high (cf. column 3, lines 13-14) compared with the doping density of the (epitaxial) body region 26 (cf. column 3, line 46).

*Mogi et al do not necessarily teach* the further limitations defined by ad (b) and (d).

*However, with regard further limitation (b)* it has long been shown that a most efficient method of making source and drain in vertical trench MOSFET devices comprises the use of a single ion beam irradiating the semiconductor material to dope source and drain simultaneously and with the same dopant as defined by the beam ions as shown by Vinson in a patent on a vertical MOSFET with groove alias trench (cf. title and abstract); while

*with regard to further limitation (d), for the specific purpose of retaining electrical symmetry (cf. column 6, line 32)*, Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer without additional doping (cf. column 3, lines 5-6 and line 24) and with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include aspects ad (b) and (d) as taught by Vinson. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include the further limitations ad (b) and (d); hence claim 14 is unpatentable over Mogi et al in view of Vinson.

*With regard to claims 15-16*: Mogi et al use arsenic as the said doping material, while the examiner takes official notice that phosphor is also standardly used for the same purpose, while having the advantage of being less toxic.

3. ***Claim 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al and Vinson as applied to claim 4 above, and further in view of Seki (5,025,293). As detailed above, claim 4, on which claim 5 depends, is unpatentable over Mogi et al in view of Vinson, neither of whom, however, necessarily teach the further limitation as defined by claim 5. *However, the use of gold, or as a non-exclusive alternative platinum*, as a dopant in semiconductor material as a material to provide generation-recombination centers *for the purpose of shortening charge carrier lifetime and thereby reducing turn-off time* has long been known in the art of semiconductor device technology, as witnessed by Seki who teach the application of either gold or platinum to facilitate recombination of electrons and holes of this purpose in a vertical MOSFET. Although the device taught by Seki et al is not a trench type vertical MOSFET the same desirability of short turn-off time qualifies as a legitimate advantage and hence said purpose is valid for Applicants' invention as well. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 4 at the time it was made so as to include the further limitation of claim 5.

4. ***Claim 9*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Mogi et al and Vinson as applied to claim 6 above, and further in view of Wolf et al (ISBN 0-

9616721-6-1). As detailed above, claim 6 (on which claim 9 depends) is unpatentable over Mogi et al in view of Vinson.

*Neither Mogi et al nor Vinson necessarily teach* the further limitation as defined by claim 9.

*However, as explained in standard textbooks such as Wolf et al, the use of silicon oxynitride as semiconductor insulation layer has long been recognized to have the following advantages:* the properties of silicon oxynitrides can be tailored, through the stoichiometric variables pertaining to the oxygen and nitrogen contents, to improve (a) thermal stability, (b) lower film stress, and (c) crack resistance.

*All of the above three advantages have relevance for the gate insulating layer in the invention by Applicants.* Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 6 so as to include the further limitation as defined by claim 9.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
February 14, 2002